In the Claims

1. (Previously Presented) An apparatus, comprising:

a substrate having at least one trench wall;

a first layer;

a second layer wherein the first layer, the second layer and a portion of the substrate form a process stack, the first and second layers being a pull back distance from the trench wall thereby forming an exposed implant region having a rounded corner between the portion of the substrate and the trench wall without the use of spacers covering the implant region; and

a dopant in the implant region having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack.

2. (Original) The apparatus according to claim 1, wherein the pull back distance is in a range from about 25 Å to about 300 Å.

3. (Original) The apparatus according to claim 1, wherein the pull back distance is substantially symmetrical about the second layer.

4. (Original) The apparatus according to claim 1, wherein the dopant in the implant region occupies the implant region in a concentration of about 1 part per million.

5. (Original) The apparatus according to claim 1, wherein the dopant has an implant energy in a preferred implant energy range from about 5 to about 25 keV.

6. (Previously Presented) An apparatus, comprising:

a substrate having at least one trench wall;

a first layer;

a second layer wherein the first layer, the second layer and a portion of the substrate form a process stack, the substrate further including a central area underneath the first layer having a

threshold voltage that is about substantially uniform, the first and second layers being a pull back distance from the trench wall thereby forming an exposed implant region having a rounded corner between the portion of the substrate and the trench wall without the use of spacers over the implant region; and

a dopant in the implant region having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack.

7. (Original) The apparatus according to claim 6, wherein the dopant in the implant region changes an electrical characteristic of the implant region thereby making a threshold voltage in the implant region about equivalent to or greater than a threshold voltage in the central area of the substrate underneath the first layer.

8. (Canceled)

9. (Previously Presented) An apparatus, comprising:

a substrate having at least one trench wall;

a first layer;

a second layer wherein the first layer, the second layer and a portion of the substrate form a process stack, the first and second layers being a pull back distance from the trench wall thereby forming an exposed implant region having a rounded corner between the portion of the substrate and the trench wall without using spacers to cover the implant region; and

a dopant in the implant region and the substrate at the at least one trench wall region wherein the implant region has the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack.

10. (Original) The apparatus according to claim 9, wherein the substrate is a P-type

substrate and the dopant is a P-type dopant.

11. (Original) The apparatus according to claim 9, wherein the substrate is an N-type substrate and the dopant is an N-type dopant.

12. (Original) The apparatus according to claim 9, wherein the dopant is one of Boron, Arsenic, Antimony, Indium, Phosphorous, and BF2.

13. (Original) The apparatus according to claim 9, wherein the dopant has an implant energy in a preferred implant energy range from about 5 to about 25 keV.

14. (Original) The apparatus according to claim 13, wherein the implant energy is in a more preferred implant energy range of less than or equal to about 10 keV.

15. (Currently Amended) An apparatus, comprising:

a substrate having at least one trench wall;

a first layer;

a second layer wherein the first layer, the second layer and a portion of the substrate form a process stack, the first and second layers being a pull back distance from the trench wall thereby forming an exposed implant region having a migration region whereby the implant region has a rounded corner between the portion of the substrate and the trench wall without the use of spacers covering the implant region; and

a dopant in the implant and migration regions ~~region~~ having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack.

16. (Original) The apparatus according to claim 1, further comprising a third layer about the process stack.

17. (Previously Presented) An apparatus, comprising:

a substrate having a surface and at least one trench wall;

an oxide layer on the substrate;

a nitride layer on the oxide layer wherein the oxide layer, the nitride layer and a portion of the substrate form a process stack extending away from the surface, the oxide layer and the nitride layer being a pull back distance from the trench wall thereby forming an exposed implant region, the pull back distance being substantially symmetrical about the nitride layer and whereby the implant region has a rounded corner between the portion of the substrate and the trench wall without the use of spacers covering the implant region; and

a dopant in the implant region thereby making a threshold voltage in the implant region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the central area of the substrate being about substantially uniform and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack.

18. (Currently Amended) The apparatus according to claim 17, ~~wherein the~~ wherein the pull back distance is in a range from about 25 Å to about 300 Å.

19. (Original) The apparatus according to claim 17, wherein the dopant is present in the substrate at the at least one trench wall.

20. (Original) The apparatus according to claim 17, wherein the at least one trench wall is angled in relation to the surface.

21. (Original) The apparatus according to claim 17, wherein the substrate further includes a corner region that comprises a part of the implant region, the corner region having a rounded contour.

22. (Original) The apparatus according to claim 17, wherein the implant region occupies a migration region adjacent to the oxide layer.

23. (Original) The apparatus according to claim 22, wherein the dopant occupies the migration region.

24. (Previously Presented) An apparatus having reduced transistor leakage attributes, comprising:

a substrate having a surface, a corner region and at least one trench wall;

an oxide layer on the substrate;

a nitride layer on the oxide layer wherein the oxide layer, the nitride layer and a portion of the substrate form a process stack extending away from the surface, the oxide layer and the nitride layer being a pull back distance in a range from about 25 Å to about 300 Å from the trench wall thereby forming an exposed implant region, the pull back distance being substantially symmetrical about the nitride layer, the corner region of the substrate comprising a part of the implant region;

whereby the implant region has a rounded corner between the portion of the substrate and the trench wall without the use of spacers covering the implant region; and

a dopant in the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the corner region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the central area of the substrate being about substantially uniform.

25. (Original) The apparatus according to claim 24, wherein the dopant is one of Boron, Arsenic, Antimony, Indium, Phosphorous and BF2.

26. (Original) The apparatus according to claim 24, wherein the corner region has a rounded contour.

27. (Original) The apparatus according to claim 24, wherein the implant region occupies a migration region adjacent to the oxide layer.

28. (Previously Presented) A transistor structure having reduced transistor leakage attributes, comprising:

a substrate having a surface, a corner region and at least one trench wall;

a transistor structure on the substrate, the transistor structure being formed from a process stack having:

an oxide layer on the substrate;

a nitride layer on the oxide layer; and

a portion of the substrate wherein the process stack extends away from the surface, the oxide layer and the nitride layer being a pull back distance in a range from about 25 Å to about 300 Å from the trench wall thereby forming an implant region, the pull back distance being substantially symmetrical about the nitride layer, the corner region of the substrate having a rounded contour and comprising a part of the implant region;

whereby the implant region has a rounded corner between the portion of the substrate and the trench wall without the use of spacers covering the implant region;

a dopant in the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the corner region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the central area of the substrate being about substantially uniform; and

a third layer forming a plug in a shallow trench isolation of the substrate.

29-57. (Canceled)

58. (Currently Amended) An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes:

a substrate having at least one trench wall;

a transistor structure on the substrate, the transistor structure formed from a process stack having:

a first layer;

a second layer;

a portion of the substrate, the first and second layers having been pulled back a pull back distance from the trench wall thereby forming an exposed implant region; [[and]]

whereby the implant region has a rounded corner between the portion of the substrate and the trench wall without the use of spacers covering the implant region; and

a dopant in the implant region having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack.

59. (Original) The electronic system according to claim 58, wherein the pull back distance is in a range from about 25 Å to about 300 Å.

60. (Previously Presented) The electronic system according to claim 58, wherein the pull back distance is substantially symmetrical about the transistor structure.

61. (Previously Presented) The electronic system according to claim 58, wherein the substrate further includes a central area underneath the transistor structure having a threshold voltage that is about substantially uniform.

62. (Previously Presented) The electronic system according to claim 61, wherein the dopant

in the implant region changes an electrical characteristic of the implant region thereby making a threshold voltage in the implant region about equivalent to or greater than a threshold voltage in the central area of the substrate underneath the transistor structure.

63. (Original) The electronic system according to claim 58, wherein the substrate further includes a corner region that comprises a part of the implant region, the corner region having a rounded contour.

64. (Previously Presented) An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes:

a substrate having at least one trench wall;

a transistor structure on the substrate, the transistor structure formed from a process stack having:

a first layer;

a second layer; and

a portion of the substrate, the first and second layers having been pulled back a pull back distance from the trench wall thereby forming an implant region;

whereby the implant region has a rounded corner between the portion of the substrate and the trench wall without the use of spacers covering the implant region; and

a dopant in the implant region and the substrate at the at least one trench wall, the implant region having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack.

65. (Original) The electronic system according to claim 64, wherein the substrate is a P-type substrate and the dopant is a P-type dopant.

66. (Currently Amended) The electronic system according to claim 64, wherein the substrate is an [[– type]] N-type substrate and the dopant is an N-type dopant.

67. (Original) The electronic system according to claim 64, wherein the dopant in the implant region is present in a thickness range from about 200 Å to about 1000 Å.

68. (Original) The electronic system according to claim 64, wherein the dopant is one of Arsenic, Antimony, Indium, Phosphorous and BF2.

69. (Original) The electronic system according to claim 64, wherein the dopant has an implant energy in a preferred implant energy range from about 5 to about 25 keV.

70. (Original) The electronic system according to claim 69, wherein the implant energy is in a more preferred implant energy range of less than or equal to about 10 keV.

71. (Original) The electronic system according to claim 64, wherein the dopant in the implant region occupies the region in a concentration of about 1 part per million.

72. (Previously Presented) An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes:

a substrate having at least one trench wall;

a transistor structure on the substrate, the transistor structure formed from a process stack having:

a first layer;

a second layer; and

a portion of the substrate, the first and second layers having been pulled back a pull back distance from the trench wall thereby forming an implant region having a migration region adjacent the transistor structure;

whereby the implant region has a rounded corner between the portion of the substrate and the trench wall without the use of spacers covering the implant region; and

a dopant in the implant region and the migration region, the implant region having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack.

73. (Previously Presented) The electronic system according to claim 72, wherein the substrate further includes a central area underneath the transistor structure having a threshold voltage that is about substantially uniform.

74. (Previously Presented) The electronic system according to claim 73, wherein the dopant in the implant region and the migration region changes an electrical characteristic of the implant region and the migration region thereby making a threshold voltage in the implant region and the migration region about equivalent to or greater than a threshold voltage in the central area of the substrate underneath the transistor structure.

75. (Currently Amended) An electronic system, comprising:

a processor; and

a memory device having reduced transistor leakage attributes coupled to the processor, wherein the memory device includes:

a substrate having a surface, a corner region and at least one trench wall;

a transistor structure on the substrate, the transistor structure formed from a process stack having:

an oxide layer on the substrate;

a nitride layer on the oxide layer; and

a portion of the substrate wherein the process stack extends away from the surface, the oxide layer and the nitride layer being a pull back distance in a range from about 25

Å to about 300 Å from the trench wall thereby forming an implant region, the pull back distance being substantially symmetrical about the nitride layer, the corner region of the substrate including a part of the implant region;

whereby the implant region has a rounded corner between the portion of the substrate and the trench wall without the use of spacers covering the implant region; and

a dopant in the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the corner region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the transistor structure, the threshold voltage of the central area of the substrate being about substantially uniform.

76. (Original) The electronic system according to claim 75, wherein the dopant is one of Boron, Arsenic, Antimony, Indium, Phosphorous and BF2.

77. (Original) The electronic system according to claim 75, wherein the corner region has a rounded contour.